

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frank Anthony Doljack et al. :
: Art Unit: 2831
Serial No.: 10/781,571 :
: Examiner: Ha, Nguyen T.
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:
For: ACTIVE BALANCING :
MODULAR CIRCUITS :

RESPONSE TO NOTICE OF NON-COMPLIANT AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

In response to the Notice of Non-Compliant Amendment dated January 8, 2007, Applicants hereby submit a corrected claim listing to replace the claim listing in Applicants previously filed Amendment submitted January 3, 2007. The claim listing includes corrected status identifiers for claims 53 and 54 in response to the Notice.

IN THE CLAIMS

1. (previously presented) A module having inductor-free circuitry for controlling voltage imbalances between a pair of capacitors connected in a series arrangement, comprising:

a first terminal configured for connection to a positive plate of the first capacitor;

a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

a third terminal configured for connection to a negative plate of the second capacitor; and

an active element integrated within the inductor-free circuitry between the first, second, and third terminals and adapted to substantially balance the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third terminals,

wherein the active element is an op amp, the op amp having an input, an output, and a feedback loop, the input being connected to two voltage dividing resistors, the output being connected to the second terminal through a current limiting resistor, wherein an end of the feedback loop is connected between the output and the current limiting resistor.

2-4. (canceled)

5. (previously presented) The module of claim 1, wherein the feedback loop includes a feedback resistor.

6. (previously presented) A module having inductor-free circuitry for controlling voltage imbalances between a pair of capacitors connected in a series arrangement, comprising:

a first terminal configured for connection to a positive plate of the first capacitor

a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

a third terminal configured for connection to a negative plate of the second capacitor; and

an active element integrated within the inductor-free circuitry between the first, second, and third terminals and adapted to substantially balance the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third terminals, wherein the active element is a switched voltage converter that incorporates a flying capacitor.

7. (canceled)

8. (original) The module of claim 1, wherein at least one of the terminals is further configured for connection to a second module having inductor-free circuitry for controlling voltage imbalances between a second pair of capacitors connected in the series arrangement.

9. (original) The module of claim 8, wherein the first and second modules' inductor-free circuitries are substantially identical.

10. (original) The module of claim 8 wherein the first and second modules' circuitry overlap upon connection to the second module.

11. (original) The module of claim 10, wherein the first and second module's circuitry overlap at one of the terminals.

12. (original) The module of claim 10, wherein the first and second modules' circuitry overlap across a common capacitor shared by the two pairs of capacitors.

13-19. (canceled)

20. (previously presented) A method for controlling voltage imbalances between a pair of capacitors connected in a series arrangement, comprising:

forming a first terminal configured for connection to a positive plate of the first capacitor;

forming a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

forming a third terminal configured for connection to a negative plate of the second capacitor; and

integrating an active element within an inductor-free circuitry between the first, second, and third terminals such that the active element substantially balances the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third terminals, wherein the active element is an op amp, the op amp having an input, an output, and a

feedback loop, wherein integrating the active element comprises:

connecting the input to two voltage dividing resistors:

connecting the output to the second terminal through a current limiting resistor; and

connecting an end of the feedback loop between the output and the current limiting resistor.

21-23. (canceled)

24. (previously presented) The method of claim 20, wherein the feedback loop includes a feedback resistor.

25. (previously presented) A method for controlling voltage

imbalances between a pair of capacitors connected in a series arrangement, comprising:

forming a first terminal configured for connection to a positive plate of the first capacitor;

forming a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

forming a third terminal configured for connection to a negative plate of the second capacitor; and

integrating an active element within an inductor-free circuitry between the first, second, and third terminals such that the active element substantially balances the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third terminals, wherein the active element is a switched voltage converter that incorporates a flying capacitor.

26. (canceled)

27. (previously presented) The method of claim 20, comprising:
- connecting at least one of the terminals to a second module having inductor-free circuitry for controlling voltage imbalances between a second pair of capacitors connected in the series arrangement.
28. (previously presented) The method of claim 27, wherein the first and second modules are substantially identical.
29. (previously presented) The method of claim 27, wherein connecting at least one of the terminals to the second module comprises:
- overlapping the first and second modules upon connection to the second module.
30. (previously presented) The method of claim 29, wherein connecting at least one of the terminals to the second module comprises:
- overlapping the first and second modules at one of the terminals.
31. (previously presented) The method of claim 29, wherein connecting at least one of the terminals to the second module comprises:
- overlapping the first and second modules across a common capacitor shared by the two pairs of capacitors.
32. (previously presented) The module of claim 1, wherein the power connections are 1) between a V+ terminal of the active element and the first terminal; and 2) between a V- terminal of the active element and the third terminal.
33. (previously presented) The module of claim 8, wherein the first and second modules' inductor-free circuitries are identical.
34. (previously presented): The module of claim 33 wherein the first and second modules' circuitry overlap upon connection to the second module.

35. (previously presented) The module of claim 34, wherein the first and second modules' circuitry overlap across a common capacitor shared by the two pairs of capacitors.

36. (previously presented) A module having inductor-free circuitry for controlling voltage imbalances between a pair of capacitors connected in a series arrangement, comprising:

a first terminal configured for connection to a positive plate of the first capacitor;

a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

a third terminal configured for connection to a negative plate of the second capacitor; and

an active element integrated within the inductor-free circuitry between the first, second, and third terminals and adapted to substantially balance the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third terminals.

37. (previously presented) A method for controlling voltage imbalances between a pair of capacitors connected in a series arrangement, comprising:

forming a first terminal configured for connection to a positive plate of the first capacitor;

forming a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor;

forming a third terminal configured for connection to a negative plate of the second capacitor; and

integrating an active element within an inductor-free circuitry between the first, second, and third terminals such that the active element substantially balances the voltage imbalances between the pair of capacitors, the active element having power connections to the first and third terminals.

38. (previously presented) An active balancing system for controlling voltages, the system comprising:

a first capacitor;

a second capacitor connected in series with the first capacitor; and

an active element connected between the first and second capacitors, the active element substantially balancing a voltage imbalance between the first and second capacitors, wherein the active element is inductor free.

39. (new) The module of claim 36, wherein the feedback loop includes a feedback resistor.

40. (new) The module of claim 36, wherein at least one of the terminals is further configured for connection to a second module having inductor-free circuitry for controlling voltage imbalances between a second pair of capacitors connected in the series arrangement.

41. (new) The module of claim 40, wherein the first and second modules' inductor-free circuitries are substantially identical.

42. (new) The module of claim 40 wherein the first and second modules' circuitry overlap upon connection to the second module.

43. (new) The module of claim 40, wherein the first and second module's circuitry overlap at one of the terminals.

44. (new) The module of claim 40, wherein the first and second modules' circuitry overlap across a common capacitor shared by the two pairs of capacitors.

45. (new) The method of claim 37, wherein the feedback loop includes a feedback resistor.

46. (new) The method of claim 37, comprising:

connecting at least one of the terminals to a second module having inductor-free circuitry for controlling voltage imbalances between a second pair of capacitors connected in the series arrangement.

47. (new) The method of claim 46, wherein the first and second modules are substantially identical.

48. (new) The method of claim 47, wherein connecting at least one of the terminals to the second module comprises:

overlapping the first and second modules upon connection to the second module.

49. (new) The method of claim 47, wherein connecting at least one of the terminals to the second module comprises:

overlapping the first and second modules at one of the terminals.

50. (new) The method of claim 49, wherein connecting at least one of the terminals to the second module comprises:

overlapping the first and second modules across a common capacitor shared by the two pairs of capacitors.

51. (new) The module of claim 36, wherein the power connections are 1) between a V+ terminal of the active element and the first terminal; and 2) between a V- terminal of the active element and the third terminal.

52. (new) The module of claim 40, wherein the first and second modules' inductor-free circuitries are identical.

53. (new) The module of claim 52 wherein the first and second modules' circuitry overlap upon connection to the second module.

54. (new) The module of claim 53, wherein the first and second modules' circuitry overlap across a common capacitor shared by the two pairs of capacitors.

Remarks

Claims 1, 5-6, 7, 8-12, 20, 24-25 and 27-54 are now pending and are believed to recite patentable subject matter.

Applicant believes that no extension of term is required and that no additional fee for claims is required. If any additional fee is required for an extension of term or claims, the Commissioner is hereby authorized to charge Deposit Account No. 01-2384.

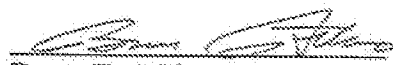
Status identifiers for claims 53 and 54 are corrected herein in response to the Notice of Non-Compliant Amendment dated January 8, 2007.

Except for correction of the status identifiers in claims 53 and 54, no changes to the claims are presented herein vis-à-vis the claims of the previously submitted Amendment dated January 3, 2007.

The Office is respectfully requested to consider the present claim listing together with the remarks submitted in the Amendment dated January 3, 2007..

Favorable action is respectfully solicited.

Respectfully Submitted,


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1		Response to Notice of Non-Compliant Amendment.PDF	333784	yes	8
Multipart Description/PDF files in .zip description					
Document Description			Start	End	
Amendment - After Non-Final Rejection			1	1	
Claims			2	8	
Applicant Arguments/Remarks Made in an Amendment			9	9	

Warnings:

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.